In the claims:

Please substitute the following full listing of claims for the claims as originally filed or most recently amended. Claims 1 - 7 are currently canceled without prejudice or disclaimer. Claims 13 - 20 have previously been canceled. Claim 8 has been rewritten in independent form.

Claims 1. - 7. (Canceled)

8. (Currently Amended) A method of adjusting carrier mobility in semiconductor devices comprising the steps of

depositing a metal or combination of metals to contact one of a first or second transistor gate structure, ~~A method as recited in claim 1~~ wherein said depositing step comprises

depositing a first metal or combination of metals to a portion of ~~said~~ gate electrode material in said first or second transistor structure to form ~~a third~~ an alloy at the lower region of the gate electrode proximate to the channel of said first or second transistor; and

depositing a second metal or combination of metals over said first or second transistor gate electrode to form ~~said~~ a first stressed alloy within said first or second transistor gate in the upper region of the gate electrode, and

alloying said metal or combination of metals and said one of a first and second transistor gate structure to form at least said first stressed alloy within said one of a first or second transistor gate whereby a first stress is created in at least one corresponding channel of first or second transistors without producing a stress in a channel of the other transistor of said first or second transistors.

9. (Currently Amended) A method as recited in claim 8 wherein said depositing step further comprises

depositing a ~~third~~ metal or combination of metals to a portion of said gate electrode material in said other transistor of said first and second ~~transistor~~ transistors to form ~~a fourth~~ an alloy at the lower region of the gate electrode proximate to the channel of said ~~second~~ other transistor; and

depositing a ~~fourth~~ metal or combination of metals over said ~~second~~ other transistor gate electrode to form ~~said second~~ a stressed alloy within said ~~second~~ other transistor gate in the upper region of the gate electrode, and

alloying said metal or combination of metals and said transistor gate structure to form at least a second stressed alloy within said transistor gate of said other transistor, whereby said second stressed alloy within said other transistor gate electrode creates a second stress ~~to~~ in ~~the~~ a channel area of said ~~second~~ other transistor.

10. (Original) A method as recited in claim 9 wherein the first stressed alloy and second stressed alloy are of opposing stresses.

11. (Original) A method as recited in claim 10 wherein the first transistor and second transistor are of opposite conductivity types.

12. (Original) A method as recited in claim 11 wherein

said first transistor is an nFET wherein said first stressed alloy is compressive creating said first stress wherein first stress is tensile, and

said second transistor is a pFET wherein said second stressed alloy is tensile creating said second stress wherein second stress is compressive.

13. - 20. (Canceled)